Implementing a Three Pin, Half-Duplex, Dual Protocol (RS-232/RS-485) Interface Using the ISL81387 or ISL41387

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Introduction

The simplest RS-232 or RS-485 bidirectional interface requires only three pins. For RS-232, those pins are the single-ended signals Transmit Data (TXD), Receive Data (RXD) and GND, whereas in the RS-485 interface, the pins are GND, and the bidirectional differential data lines Data+ and Data-. A three pin RS-485 interface requires a half duplex configuration where the transmitter (Tx) and receiver (Rx) terminals of the same polarity (inverting or non-inverting) are connected together, as shown in Figure 1.

Many applications (e.g., single board computers) need flexibility in defining the protocol of a port. Dual protocol ICs are ideal for this task, as the user can switch between the protocols (RS-232 and RS-485) at will, but it isn't always obvious how to implement the desired configuration.

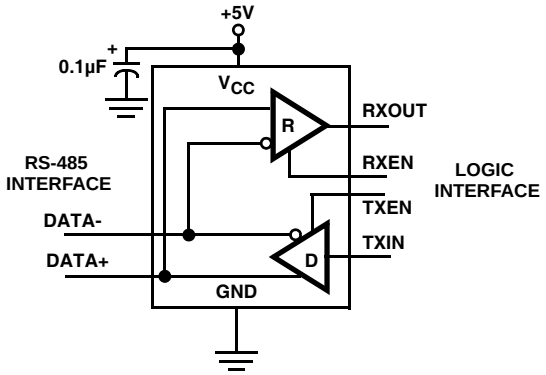

FIGURE 1. STANDARD RS-485 HALF DUPLEX TRANSCEIVER

Understanding the ISL81387, ISL41387

Figure 2 details the basic ISL81387 and ISL41387 architecture. As you can see, the two Rx input pins (A and B) are shared between the differential RS-485 Rx, and two single-ended RS-232 Rx. Likewise, the two Tx output pins (Y and Z) are shared between the differential RS-485 Tx, and the two RS-232 Tx. In most RS-232 modes, all (two of each) of the single ended transmitters and receivers are enabled. This can cause some issues which will be described in the next section.

Note: The ISL81387, ISL41387 don't follow the standard convention where A and Y are the noninverting RS-485 signals, and where B and Z are the inverting signals. Use care to ensure that the ISL81387, ISL41387 signals match the polarity of the bus signals to which they connect.

The 485/$\overline{232}$ pin selects the bus protocol, while the combined states of the DEN, RXEN, and ON pins not only control whether the Rx and Tx outputs are enabled, but they also set the ISL81387, ISL41387's sub-mode (e.g., SHDN, loopback, etc.). One of these sub-modes is particularly useful for this three pin half duplex application, as will be shown in a later section.

The D_Z/SLEW pin is the Z Transmitter input for RS-232 mode, or it selects the Tx output slew rate (fast or medium) in RS-485 mode. Drive the SLEW pin high for RS-485 data rates greater than 800kbps, or drive it low for data rates of 800kbps or less.

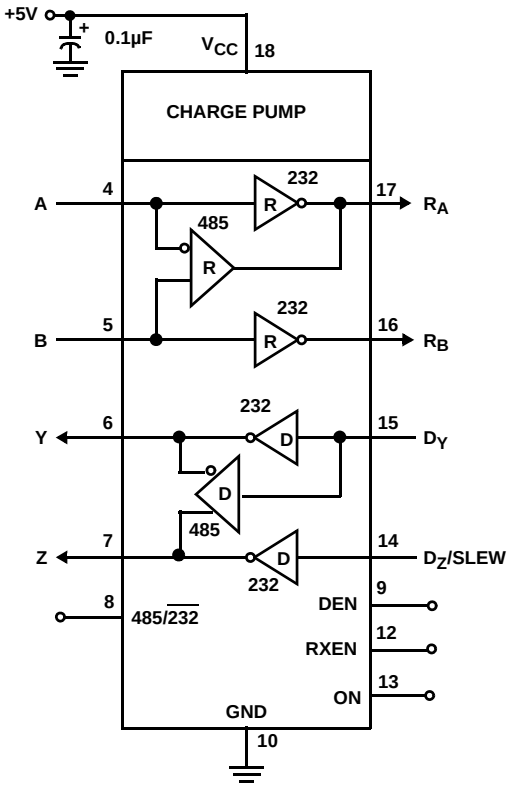

FIGURE 2. ISL81387, ISL41387 FUNCTIONAL DIAGRAM

Configuring the ISL81387, ISL41387 for RS-485 Half Duplex Mode

Focusing on the RS-485 protocol, it's not unreasonable to think that you might be able to use the ISL81387, ISL41387 internal loopback mode to achieve half duplex functionality. In reality, the Rx used for the loopback function is not an RS-485/RS-422 compatible Rx, so it doesn't operate properly when receiving RS-485/RS-422 compliant data streams.

Nevertheless, it is a simple matter to externally connect the ISL81387, ISL41387 for half duplex operation. One simply shorts the noninverting Tx output and Rx input pins (pins 5 and 7) together, and shorts the inverting Tx output and Rx input pins (pins 4 and 6) together, as shown in Figure 3 for the ISL81387. The internal RS-232 Tx and Rx are all

disabled in RS-485 mode, so they have no impact on RS-485 operation. The Tx data for transmission is applied to the DY input (pin 15), and the received data is read via the RA output (pin 17). ON, RXEN, DEN, and 485/$\overline{232}$ all connect to a “Logic 1”, as shown in line 8 of Table 1, for a transceiver with an enabled Rx to echo back the TXD.

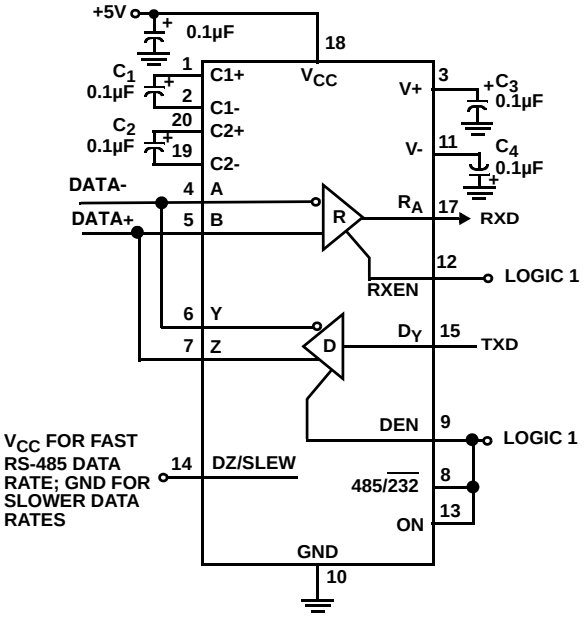

FIGURE 3. ISL81387 CONFIGURED FOR HALF-DUPLEX RS-485 OPERATION

But what happens when you switch the ISL81387, ISL41387 to RS-232 mode? Figure 4 illustrates the enabled functions and the connections in this instance. As you can see, each Rx input shorts to a Tx output, and because both Tx outputs enable in unison, data reception and transmission must be mutually exclusive. Even if this was acceptable, the RS- 232 Tx driven by the TXD signal (per the Figure 3 RS-485 I/O definition) is externally shorted to the Rx that outputs the RXD signal. Since RS-232 ports expect TXD and RXD to be separate connector pins (because there is no requirement that the Tx and Rx on the other end of the cable be tri-statable) the RS-232 side TXD or RXD must be routed to the other Tx or Rx. This could be accomplished using external switches on the logic side, but needless to say, making it work would be a mess at best.

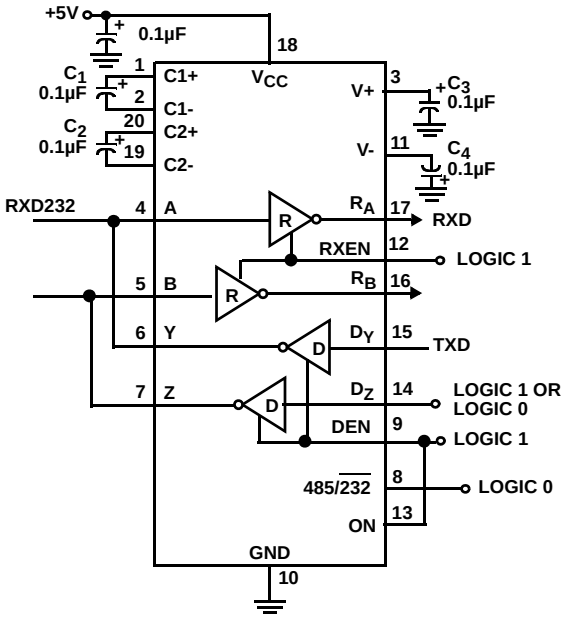

FIGURE 4. RS-232 CONNECTIONS WHEN ISL81387 IS CONFIGURED FOR HALF DUPLEX 485 MODE

Special Mode Solves the Problems

The ISL81387, ISL41387 includes a mode specifically designed for this application. In this mode, only one Rx and one Tx enable in RS-232 mode, and the enabled devices are the ones that don’t share bus pins (see Figure 5) therefore, simultaneous transmission and reception is possible. Setting ON = DEN = 485/$\overline{232}$ = Logic 0, and RXEN = Logic 1 selects this single transceiver mode (see Table 1, line 3).

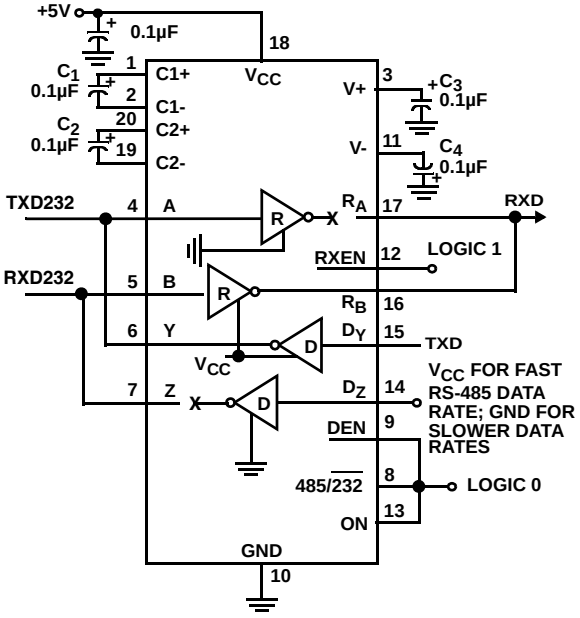

FIGURE 5. RS-232 CONNECTIONS WITH ISL81387 IN SINGLE TRANSCEIVER MODE AND EXTERNALLY CONNECTED FOR HALF DUPLEX

TABLE 1. EXCERPT FROM THE ISL81387 FUNCTION TABLE IN THE ISL81387, ISL41387 DATA SHEET

LINE NUMBER	INPUTS					RECEIVER OUTPUTS		DRIVER OUTPUTS		COMMENTS	MODE
	485/$\overline{232}$	ON	RXEN	DEN	SLEW	R_A	R_B	Y	Z		
1	0	1	0	0	NA	High-Z	High-Z	High-Z	High-Z	Disabled Tx and Rx	RS-232
2	0	0	0	1	NA	High-Z	High-Z	ON	High-Z	Single Tx Mode	RS-232
3	0	0	1	0	NA	High-Z	ON	ON	High-Z	Single Transceiver Mode	RS-232
4	0	0	1	1	NA	ON	ON	ON	ON	Loopback w/ 2 Transceivers	RS-232
5	X	0	0	0	X	High-Z	High-Z	High-Z	High-Z	Shutdown Mode	Shutdown
6	1	X	0	1	1/0	High-Z	High-Z	ON	ON	Rx Disabled	RS-485
7	1	X	1	0	X	ON	High-Z	High-Z	High-Z	Tx Disabled	RS-485
8	1	1	1	1	1/0	ON	High-Z	ON	ON	Rx Enabled for Tx Echo	RS-485
9	1	0	1	1	1/0	ON	High-Z	ON	ON	RS-485 Loopback	RS-485

As with the RS-485 mode, the Tx input is DY (pin 15), so the TXD input connection is the same for both modes. However, unlike the RS-485 mode that uses RA to output the received data, the single transceiver RS-232 mode outputs received data on the RB output. The simple solution to this quandary is to connect RA and RB together, so the RX data is read from the proper output in either mode. This works because RB is disabled in RS-485 mode, while conversely RA is disabled in this single transceiver RS-232 mode, so the two Rx outputs are never enabled at the same time (see Table 1, lines 3 and 8). The unused DZ/SLEW pin should be connected to V_{CC} or GND, depending on the slew rate required for the RS-485 data rate.

Note that in this RS-232 mode, DEN and RXEN no longer directly control the Tx and Rx enables. If DEN switches to a Logic 1, then both RS-232 Tx enable (see Table 1, line 4) in loopback mode, while changing RXEN to a Logic 0 sends the ISL81387, ISL41387 into the low power shutdown state (see Table 1 line 5).

If just an RS-232 Rx enable function is desired (i.e., Tx is always enabled), this can be accomplished by driving DEN high at the same time that RXEN is driven low (i.e., DEN is inverted from RXEN, see Table 1 line 2).

Single transceiver mode doesn't provide for separate control of the Tx enable, so if the RS-232 Tx must be disabled, the only way to accomplish this is to also disable the Rx. This can be accomplished by forcing the ISL81387, ISL41387 into SHDN (simply drive RXEN low, see Table 1 line 5), or by driving ON high while simultaneously driving RXEN and DEN low (see Table 1,line 1). Note that SHDN turns off the charge pumps, so the reenable times are longer than the enable times if just the Tx and Rx are disabled.

To switch to the standard RS-485 mode, simply drive the 485/$\overline{232}$ and ON pins high (see Table 1, lines 6, 7, and 8). DEN and RXEN now control the enable states of the Tx and Rx as would be expected (see Table 1, lines 6 and 7).

Simplified Connections

Figure 6 shows the simplest connections to achieve the three-pin, half duplex configuration. With these connections, the ISL81387, ISL41387 operates in one of only three modes: RS-232 single transceiver, RS-485 Transmit, RS-485 receive (lines 3, 6, and 7 in Table 1). If the RS-485 mode requires echo back during transmission (i.e., Rx always enabled), simply strap RXEN high, and the ISL81387, ISL41387 now operates in only two modes (lines 3 and 8 in Table 1).

The simplified configuration's main advantage is that the logic side interface requires only four I/O pins. If SHDN or loopback modes are needed, then more I/O pins must be dedicated to controlling the ISL81387, ISL41387.

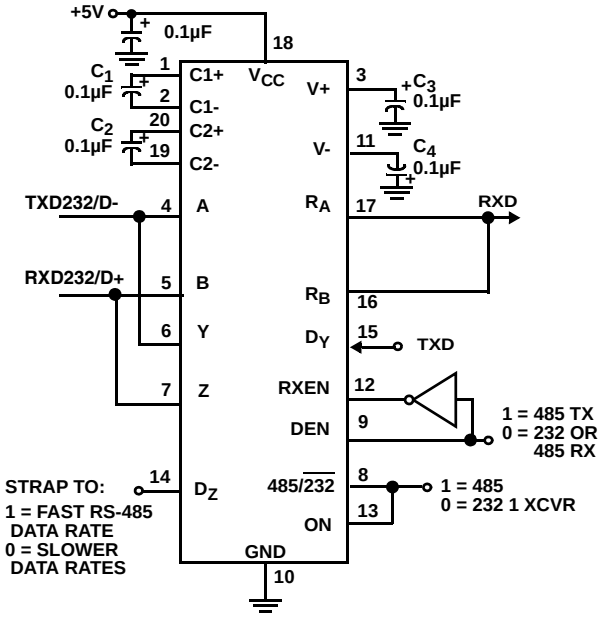

FIGURE 6. SIMPLEST CONNECTIONS FOR THREE PIN HALF DUPLEX DUAL PROTOCOL OPERATION

SHDN and Loopback Modes of Operation

SHDN and loopback are useful modes of operation. SHDN puts the ISL81387, ISL41387 into their lowest power mode, while loopback routes the Tx outputs back through the Rx (i.e., returns TXD on RXD) to allow some level of I/O port self test capability. Unfortunately, the half duplex external connections preclude utilizing loopback in RS-232 mode.

Adding just the SHDN mode is easy for either protocol. The only change required to Figure 6 is to connect an I/O pin to RXEN, rather than inverting it from DEN. SHDN is invoked by driving ON, RXEN, and DEN low, as shown in Table 1, line 5.

Adding loopback to RS-485 mode requires one more I/O pin to independently drive the ON input (so a total of 6 I/O pins for two protocols with SHDN and RS-485 loopback). With the 485/$\overline{232}$ pin high, driving ON low with DEN and RXEN high enables loopback (see Table 1, line 9).

Advantages of Using the ISL41387

Choosing the ISL41387, QFN version offers even more advantages, not the least of which is the small 6mmx6mm footprint. This version also offers an $\overline{\text{RXEN}}$ pin, which is an active low version of the RXEN pin. When implementing the circuit in Figure 6, one simply connects $\overline{\text{RXEN}}$ (QFN pin 17) and DEN together (with RXEN strapped to GND) to eliminate the external inverter. Another advantage is the built-in level shifter that is extremely useful if the logic ICs (UART, microcontroller, etc.) are powered by a supply voltage lower than the 5V supply of the ISL41387. Simply tying the ISL41387's V_L pin (QFN pin 31) to the lower supply voltage shifts the logic pin input thresholds and output voltages to values compatible with that lower supply voltage. A third, slower (115kbps) RS-485 speed option is also available on the ISL41387. This option uses even slower edge rates than the medium speed version, for EMI sensitive designs, or to allow longer bus lengths, or to minimize the risk of termination issues on slower data rate networks.

For more information on all of these special features, please refer to the ISL81387, ISL41387 data sheet.